# Power Aware Computing and Communications (PAC/C)

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# System Performance Limited by Power

- Satellites, UAVs, missiles and micro-sensor systems limited by onboard processing
  - size, weight, area, power limitations
  - potential energy savings for burst and selective processing not realizable

# Portable Power

- Portable systems require expensive, disposable batteries
  - circuits are not always power efficient
  - must prepare for worst case

- Current example: Reconn mission
  - manpower: 3-man, 3-5 days
  - energy source: 59 batteries
  - costs: 45.5 pounds

# PAC/C Vision

- The intelligent management of energy and energy distribution
  - <u>minimum</u> power required to complete a mission / task
  - empower exploration of new mission opportunities

- Power a "first class citizen" right along with performance

# Goals

Provide an <u>integrated</u> software / hardware technology suite with the potential to reduce power requirements by 100X - 1000X in (energy * delay) or performance / watt when compared to technology using conventional approaches

# PAC/C Approach
## Power Management at all levels

Protocols

Distributed Arithmetic

$V_{dd}$ Scaling

Clock Gating

Compilers/OS
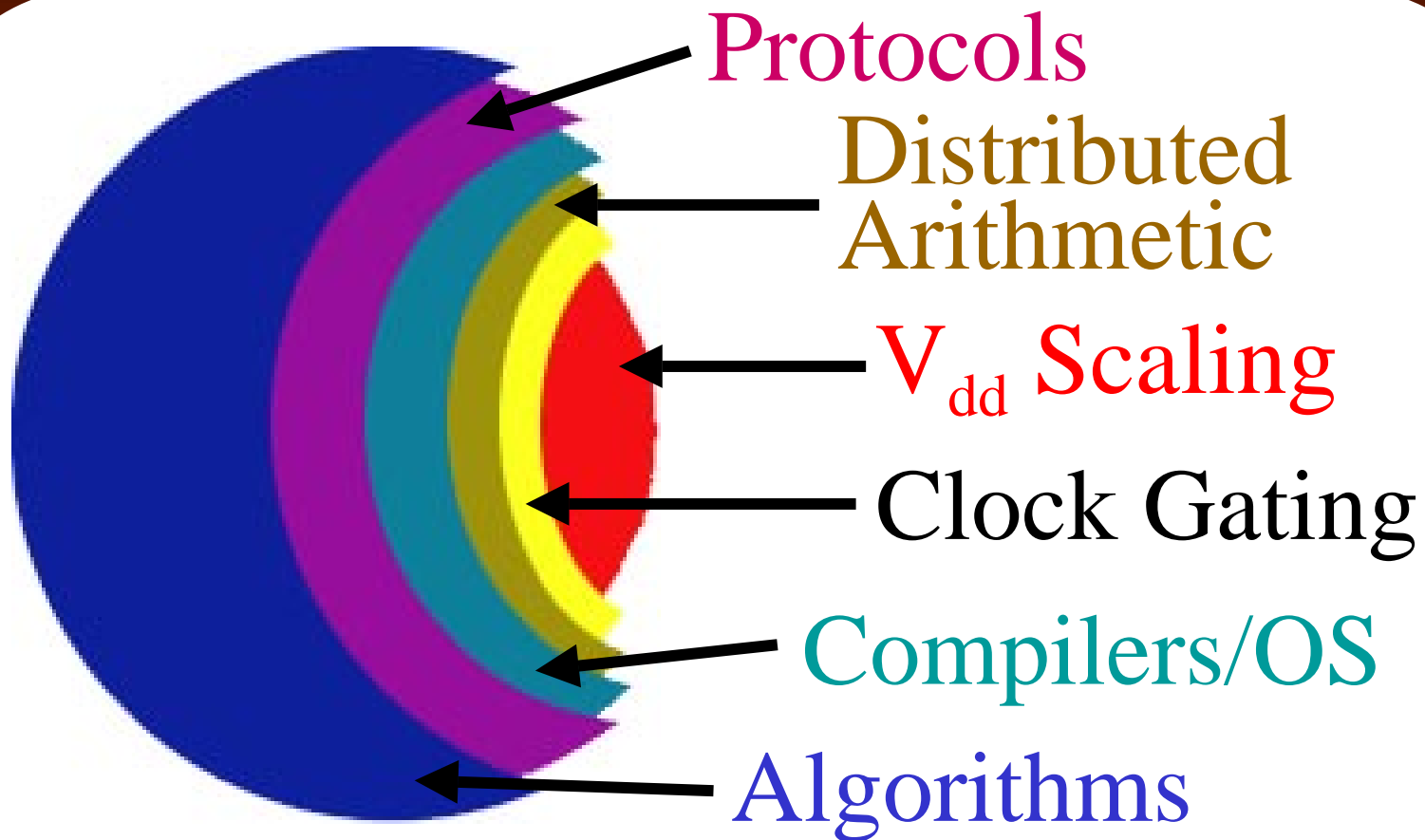
Algorithms

# Application Level

- Power-aware
  - algorithms
  - protocols

- Comprehensible, programmable power management and partitioning

- Tradeoff: compute/communicate
  - Quality-of-service demands

# System Balance

bps

MIPS

1 bit

300 ops

**Source: Brodersen (Berkeley)**
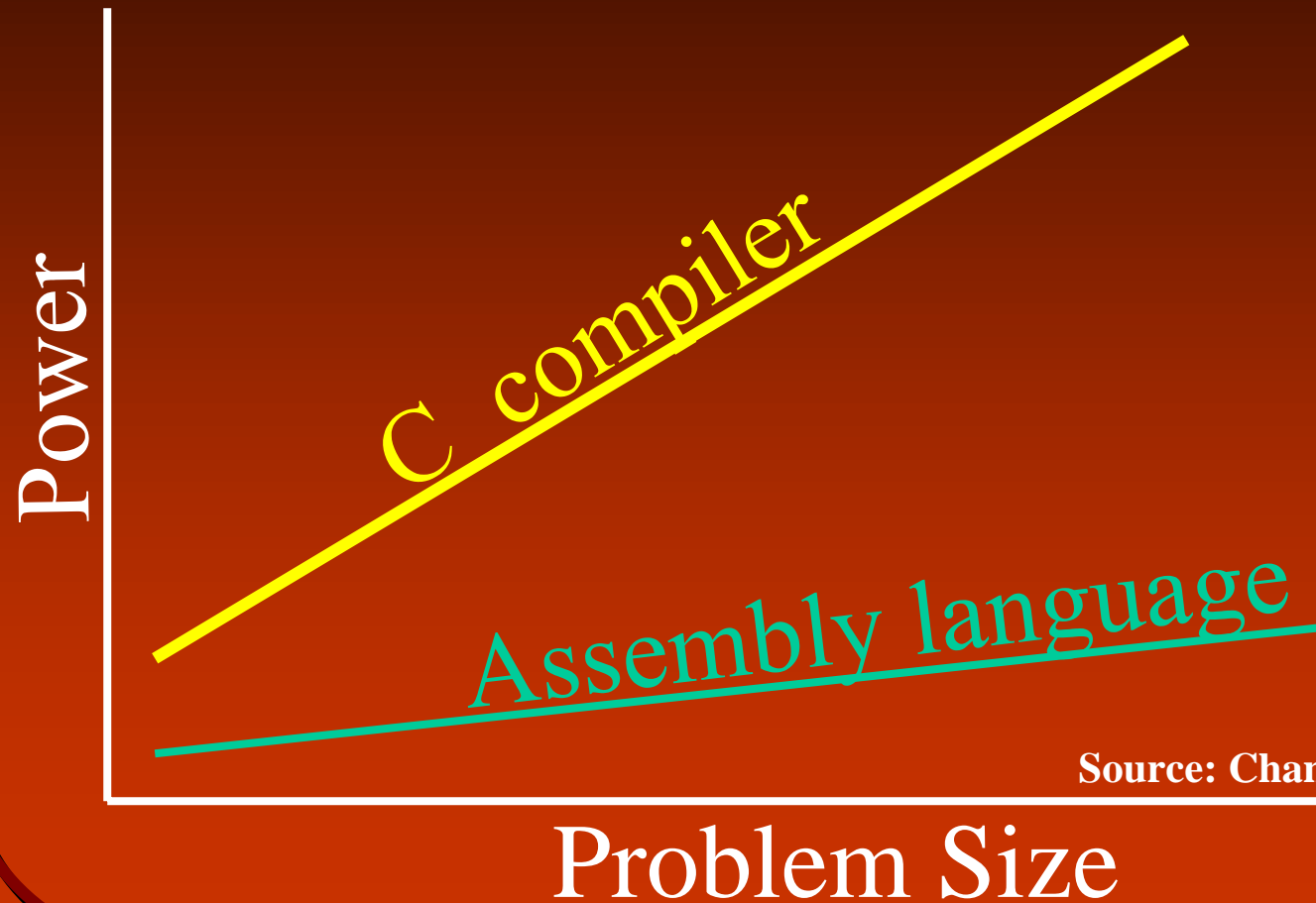
# Multi-Scale Processing

# System and Architecture Level

- Power-aware compilers, middleware, libraries and OS
- Architectural approaches
- Dynamic voltage and frequency scaling
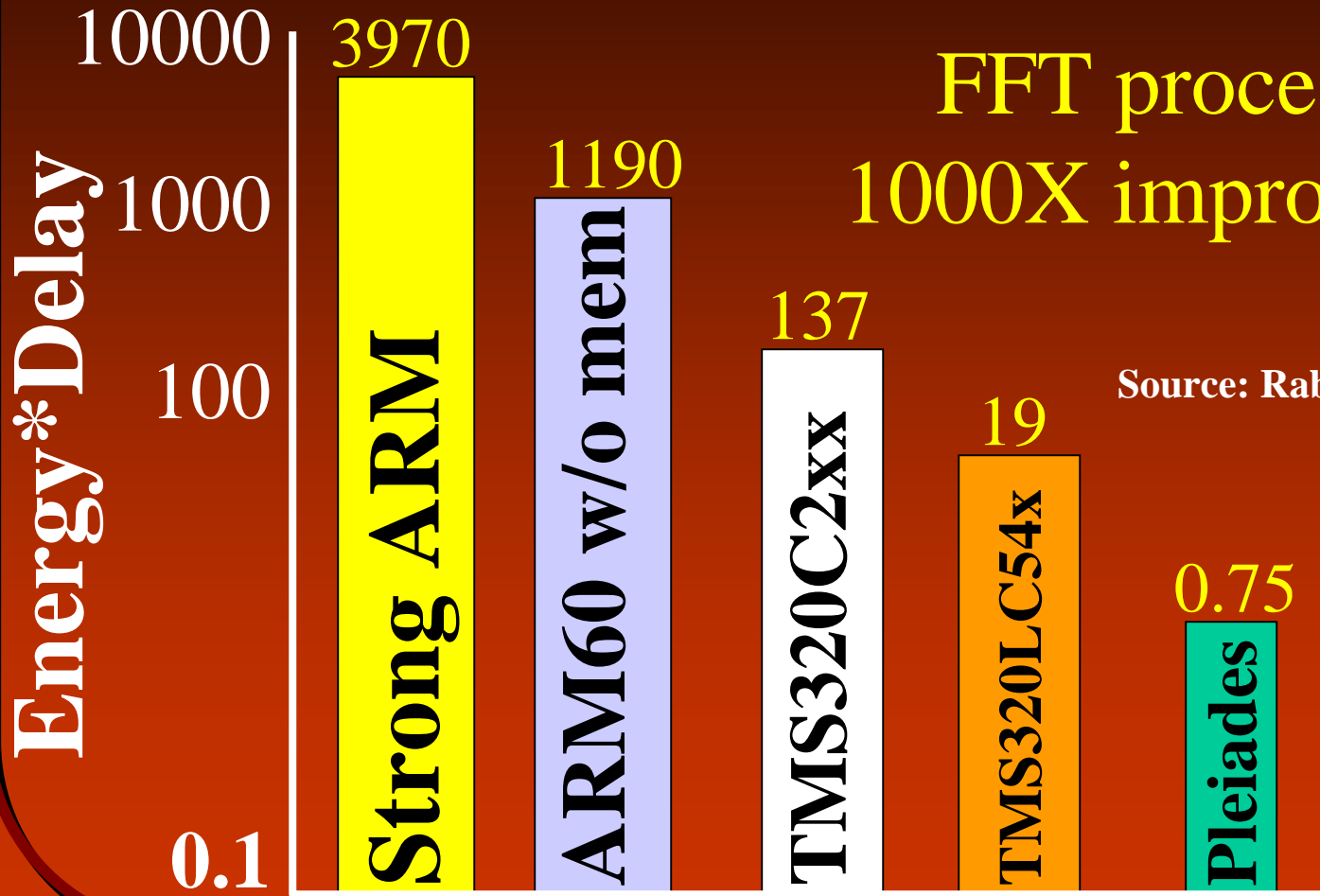- Power-aware CAD tools

# Compilation



Power

C compiler

Assembly language

Problem Size

Source: Chandrakasan (MIT)

# Dynamic V/freq

FFT processing
1000X improvement

**Source: Rabaey (Berkeley)**

Energy*Delay

- 10000
- 1000
- 100
- 0.1

- Strong ARM — 3970
- ARM60 w/o mem — 1190
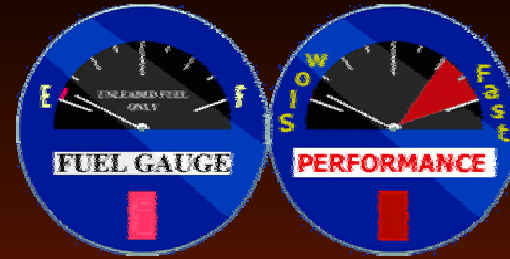- TMS320C2xx — 137
- TMS320LC54x — 19
- Pleiades — 0.75

# System Integration, Experiments and Benchmarks

- Application/system-level power aware integration

- Benchmarking, experimentation, and downselect

- Demonstrations of 10X, 100X, and 500X power reductions

# Impact

- Enable "performance on demand"
- Generic solutions
- Exploit energy saving features in existing devices
- Enable new missions/capabilities
- Technology also applicable to "low-power" systems

# Upcoming BAA

- 4QFY99 (tentative)

- Focusing on exploiting power-aware mechanisms in existing devices using compilation, algorithms and middleware

- Development of PAC/C benchmarks

# PAC/C

"JIP: Just In time Power"
The *right* power at the *right* place at the *right* time