Advanced Microelectronics

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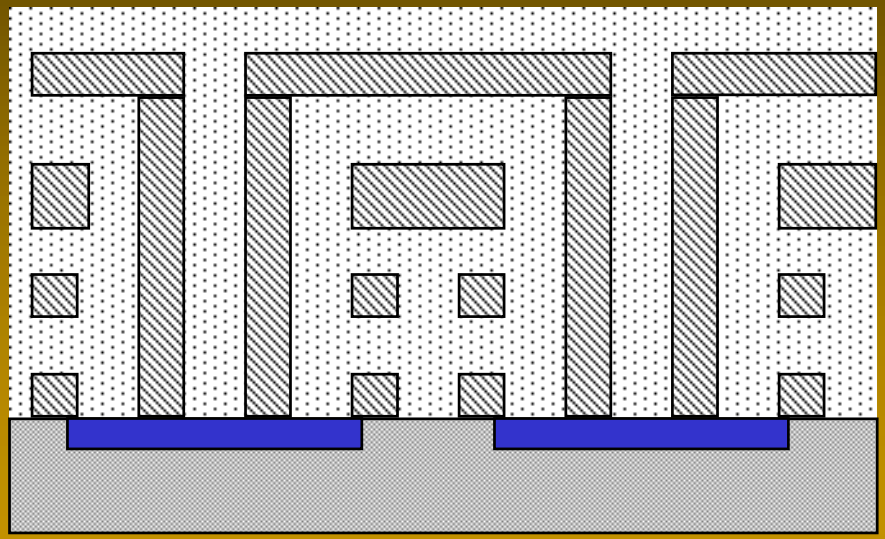
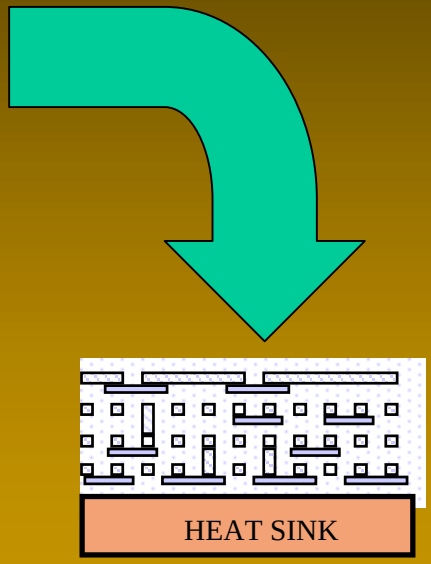
Flow of Talk

- Overview
- 25nm Transistors
- Vertical Devices
- 3D Integration
- Circuits and Structures

Terascale Integration

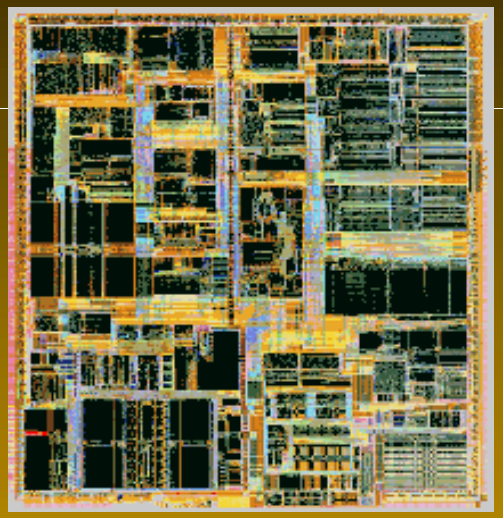
2D Transistors

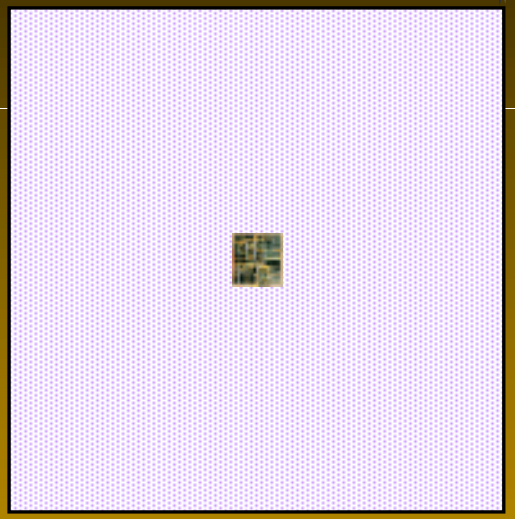




3D Si Circuits

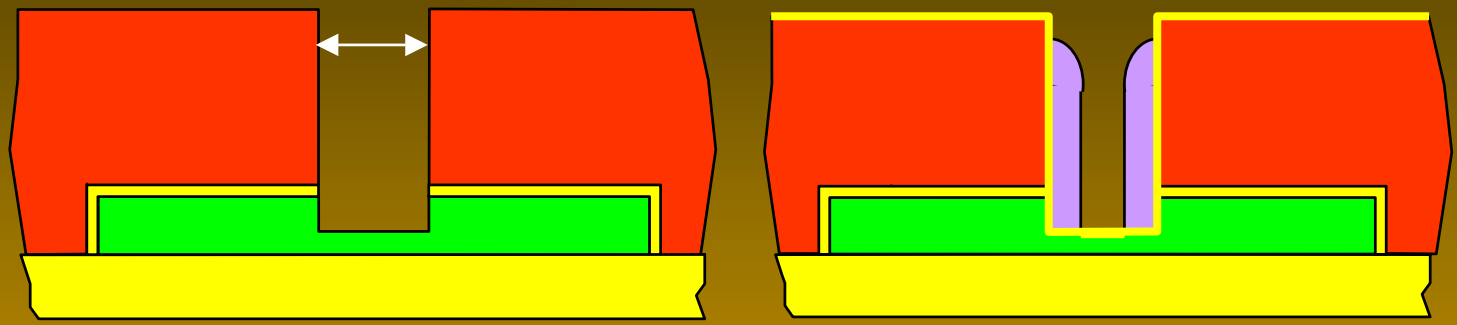
Design Opportunity





100s of billions of 25nm transistors available for design of monolithic electronic systems

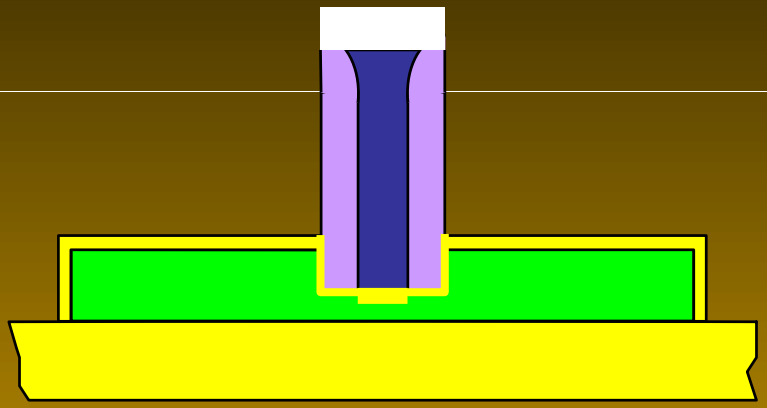
Silicon Slot FETs

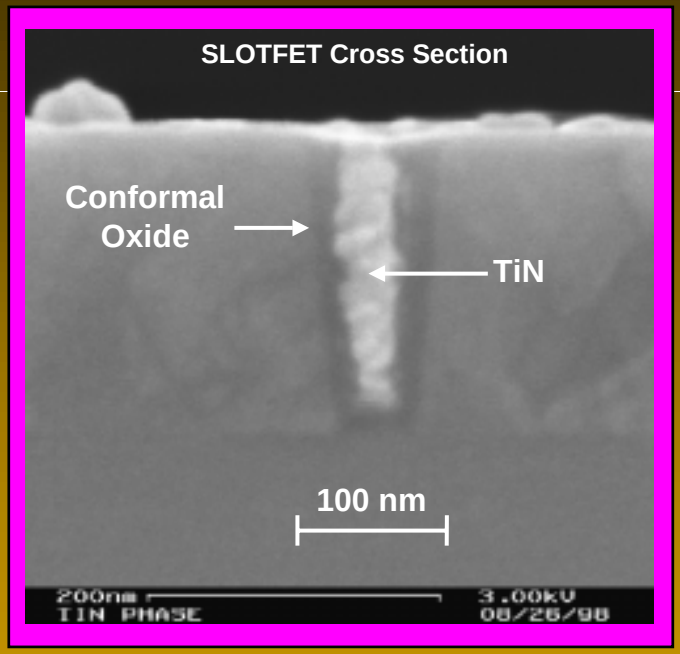


1. Etch slot

2. Spacer and Gate Ox

Silicon Slot FETs

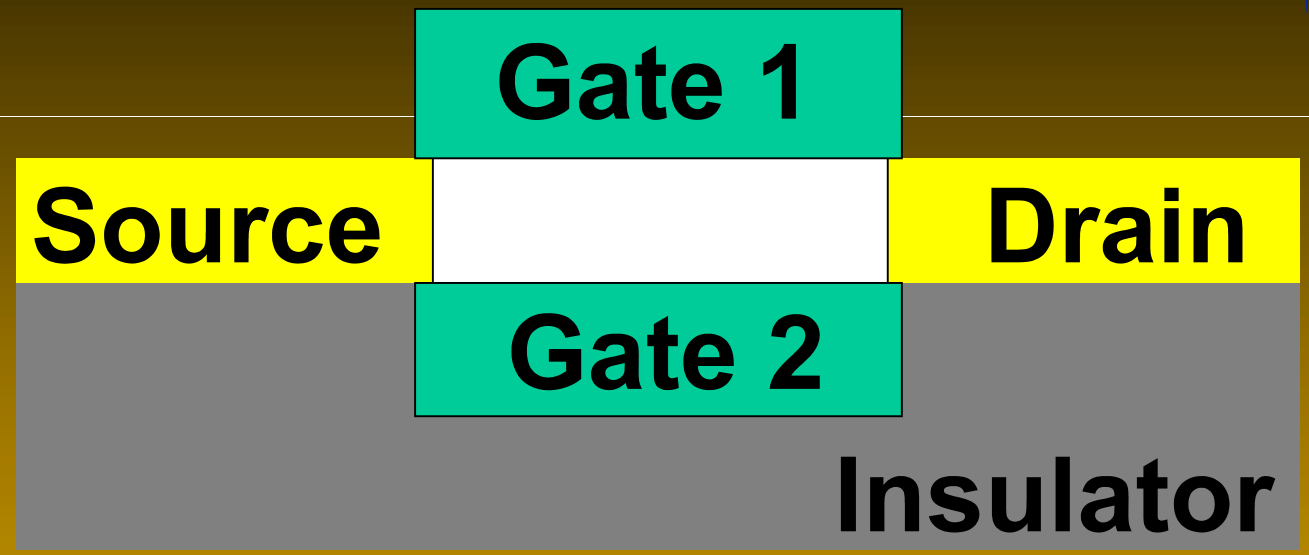




3. Gate electrode and junctions

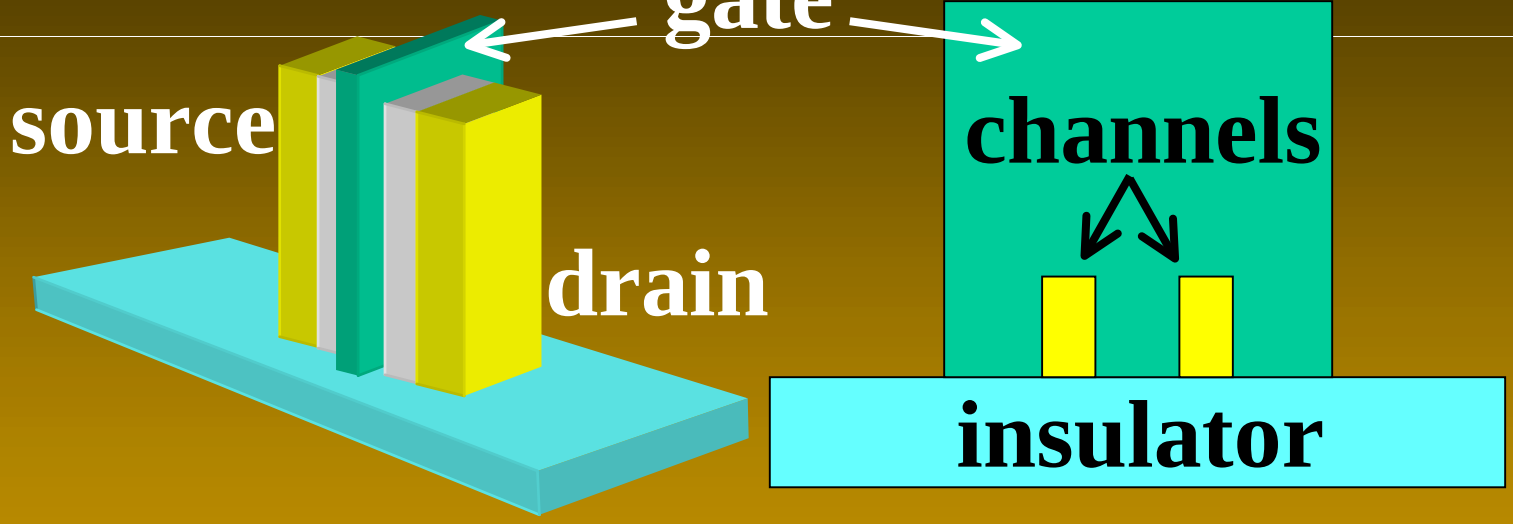
Slot FETs functional

Planar Double Gate



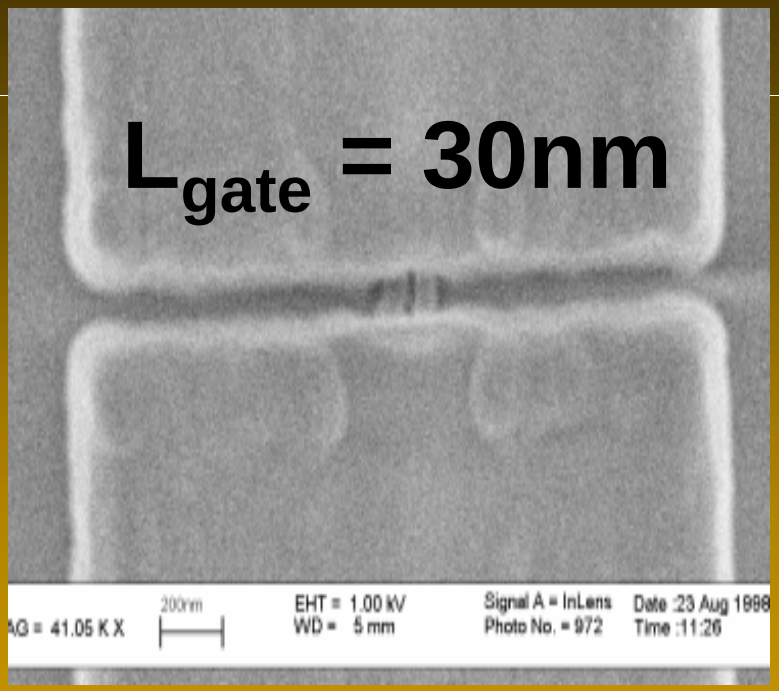
Simple device concept, difficult to self-align gates

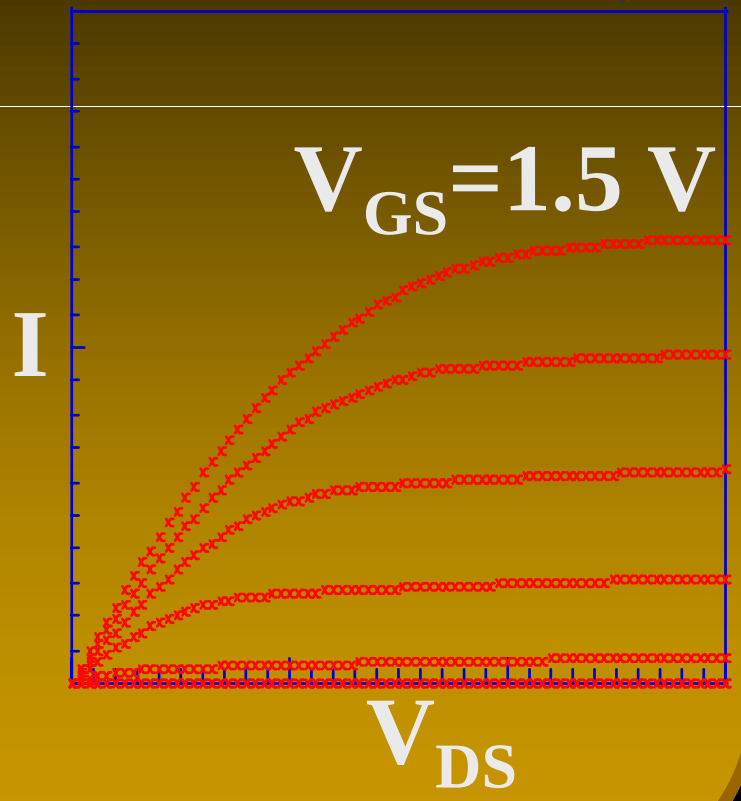
Folded Channel FET



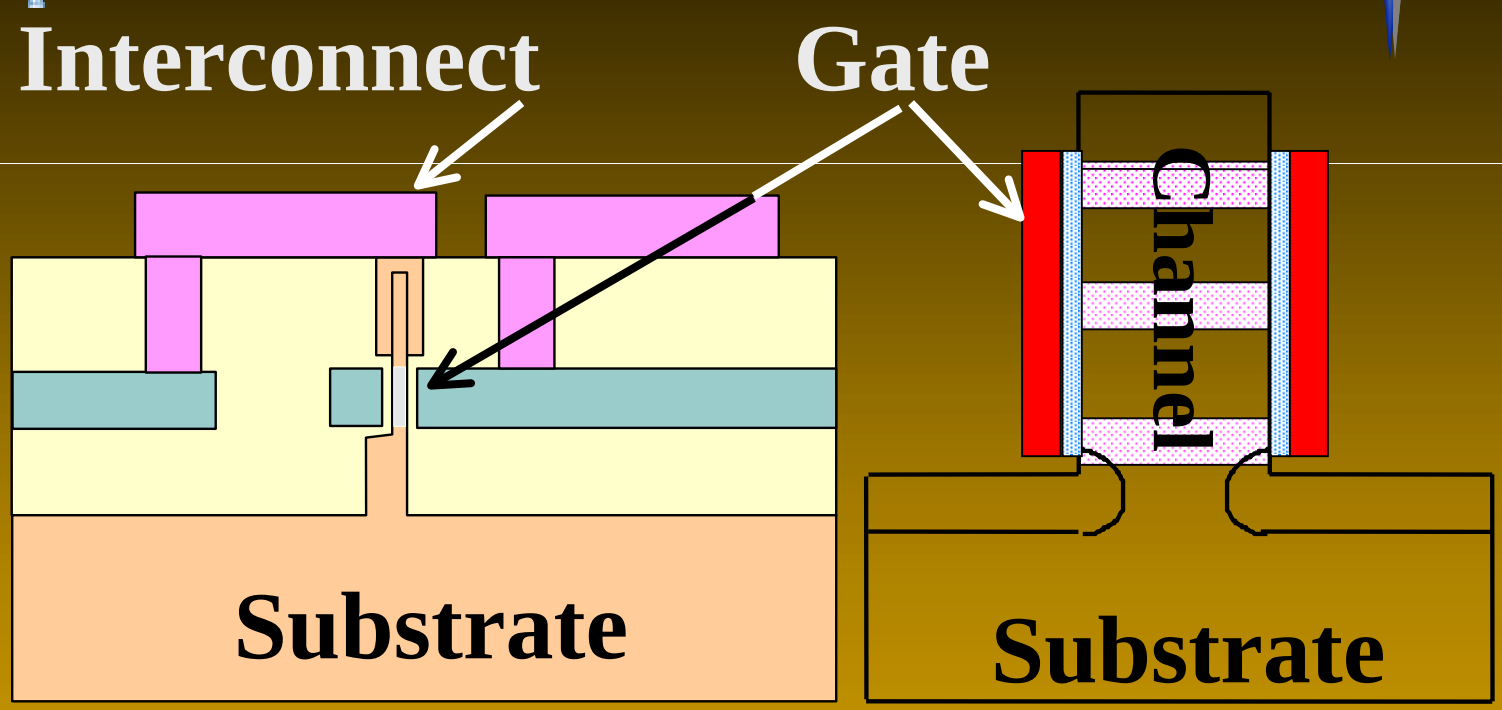
Manufacturable double gate transistor

Double Gate FET



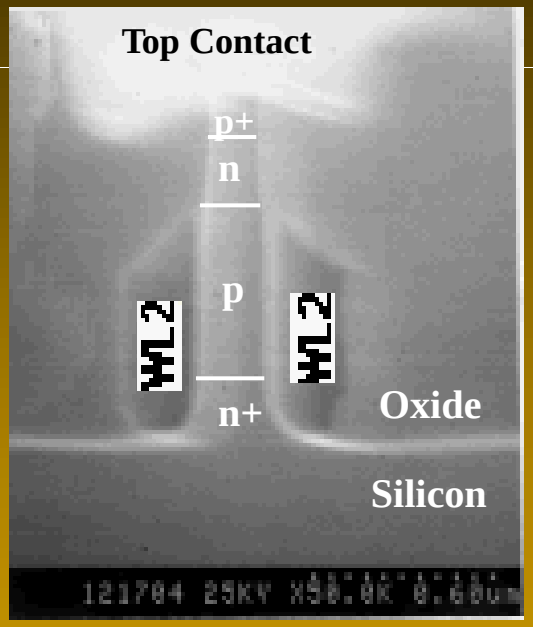


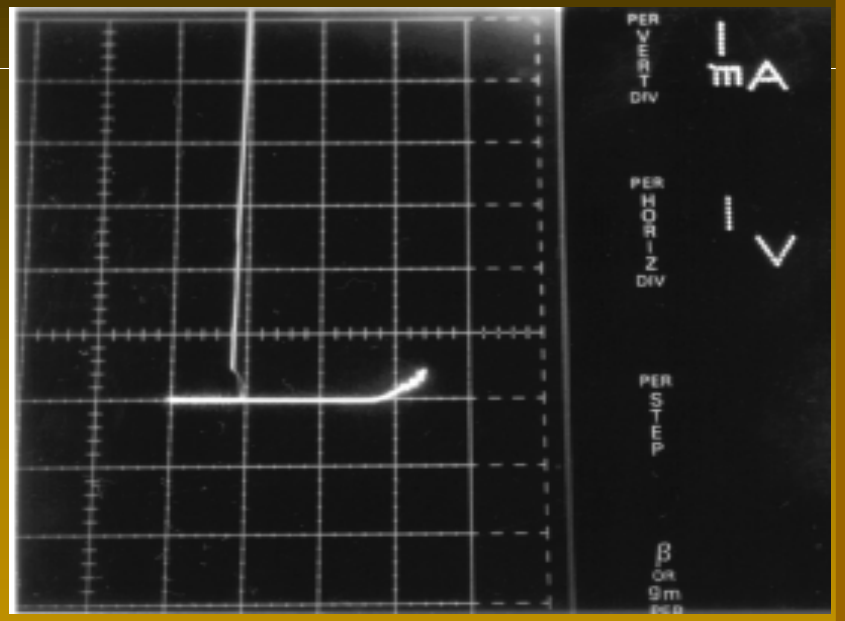
Vertical Devices



Channel engineering and greater functionality per area

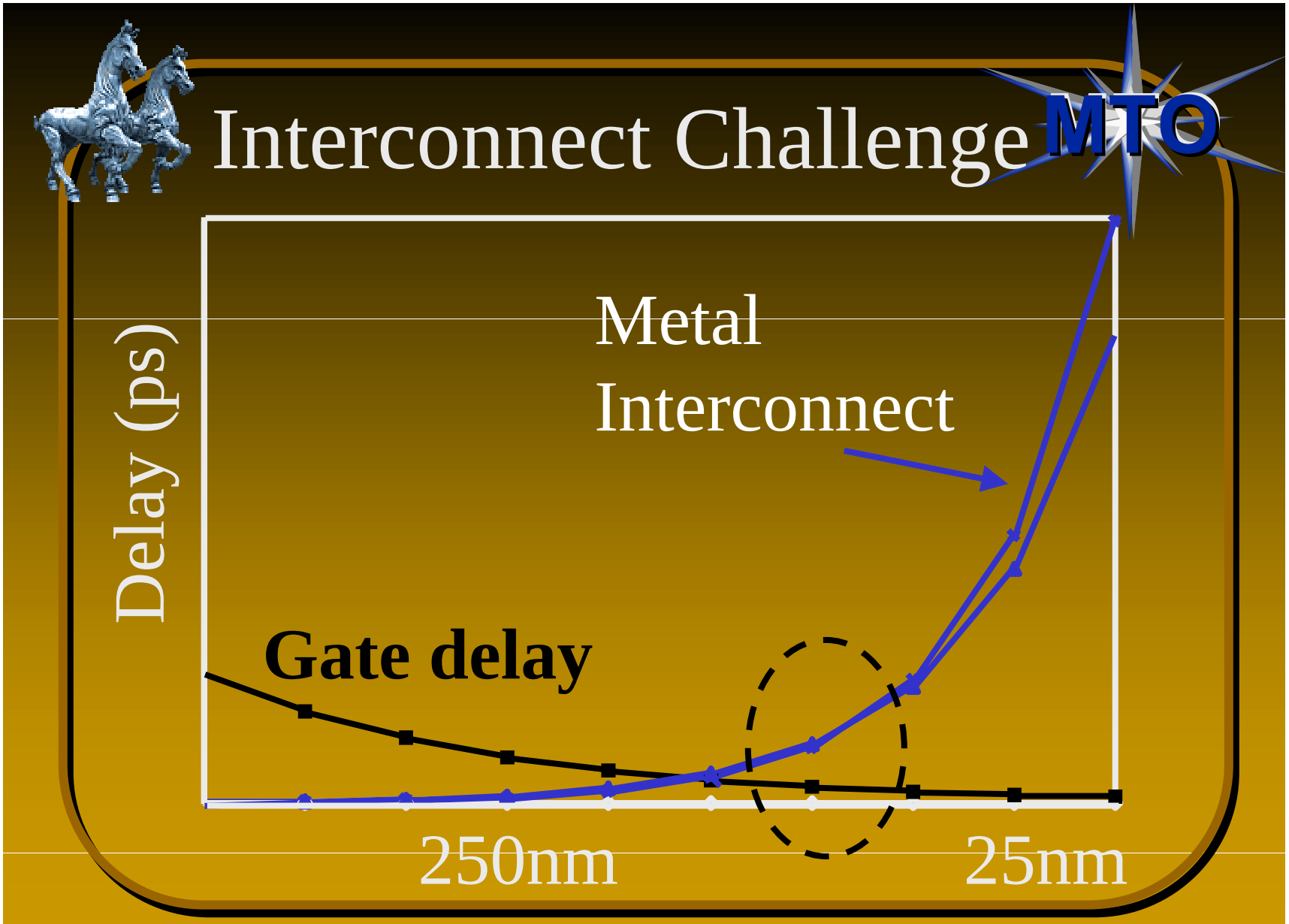
Vertical SRAM



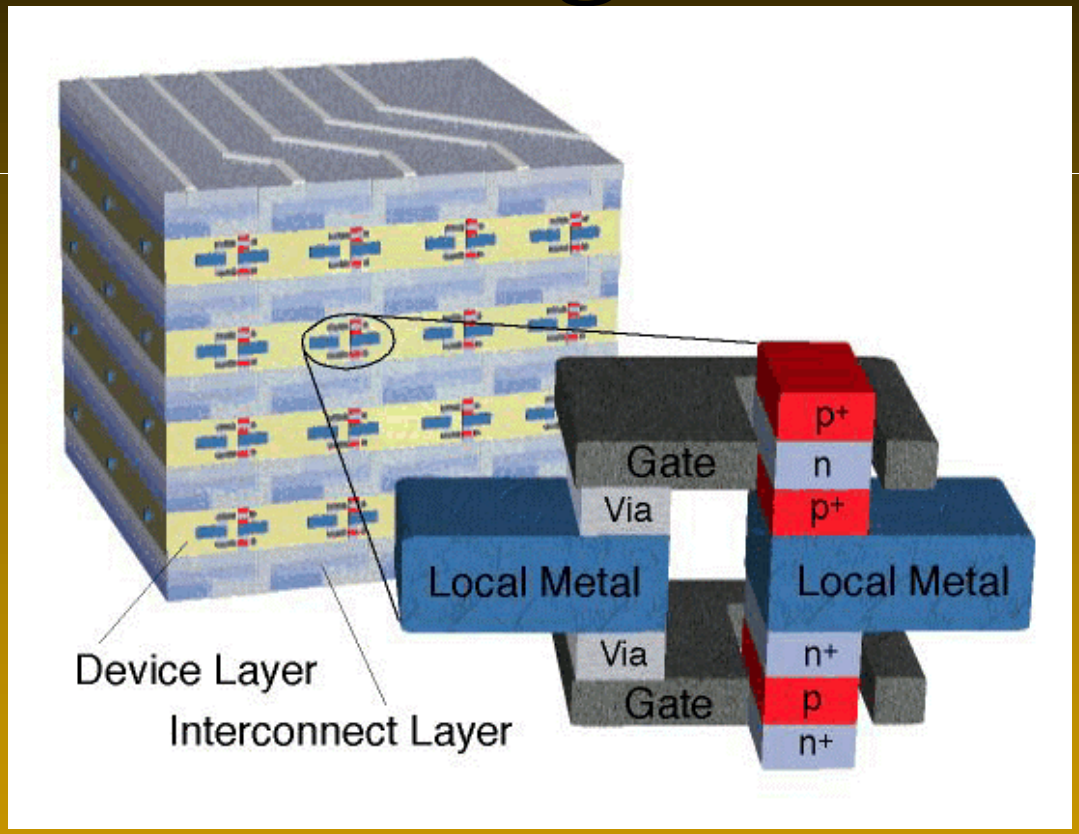


Compact, low leakage, latching

Interconnect Challenge

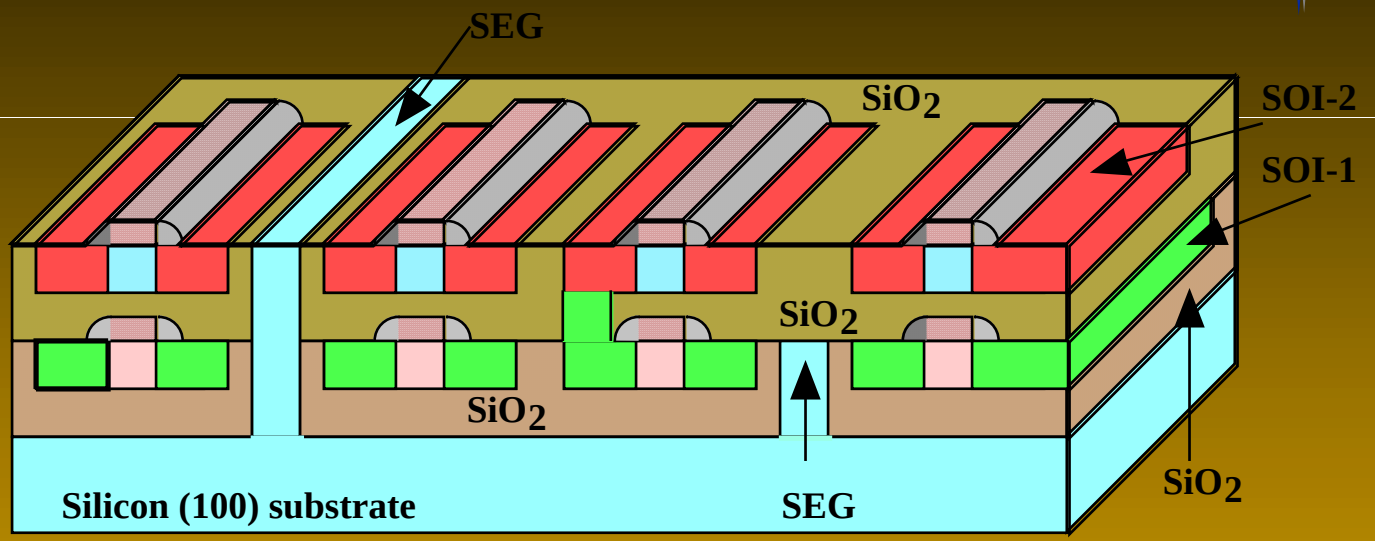


3D Integration



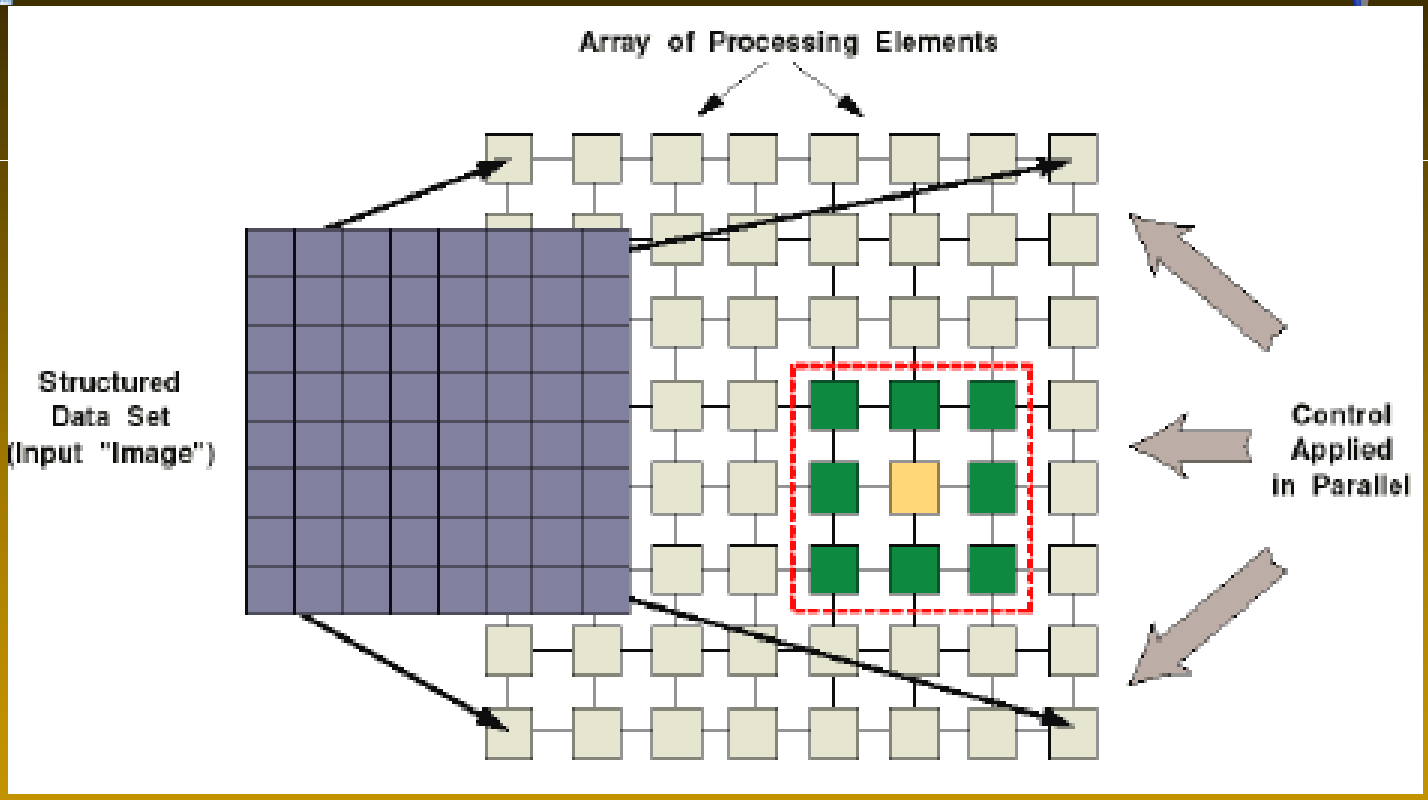
Integrated circuit on multiple layers

Multiple Si Layers



ELO/CMP demonstrated for 2 layers with low leakage transistors

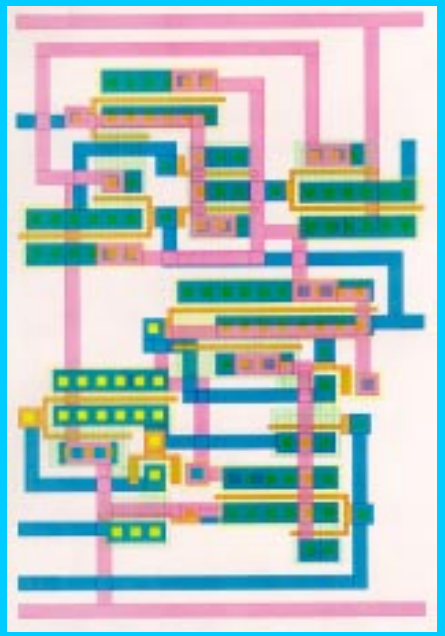
Pixel Processor



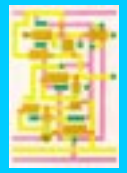
Local comm., constrained area

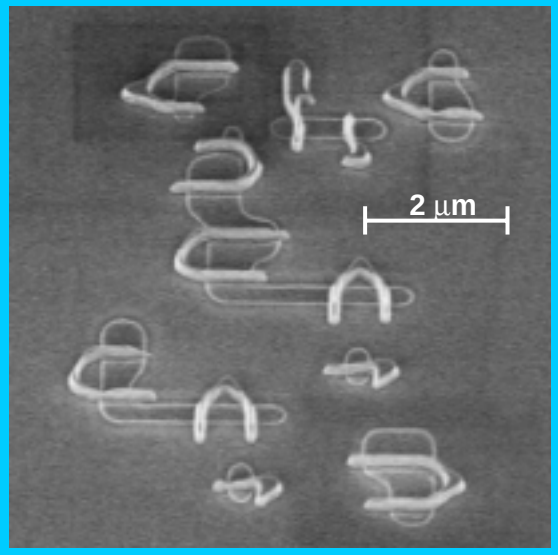
25nm Circuit Demo

250nm



25nm





Design rules for 25nm process

Summary

- 25nm transistors work!
- Vertical devices have functionality/area advantages
- Moving toward integration and circuit experiments