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Teleprompter Script for Dr. Michael Fritze, Program Manager,  
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"Ultra-Low Power Digital Electronics"

» **MICHAEL FRITZE:**

What if power density was not the key factor limiting progress for advanced electronic systems?

What would the implications be for Department of Defense?

*This is a vision with potentially revolutionary consequences!*

Imagine a network of unattended sensors deployed in a critical battle-space which could run indefinitely using on-board or scavenged power.

What new missions could this enable?

Imagine a fully autonomous unmanned air vehicle navigating by processing visual input, with no more power draw than is required today.

Imagine space-based assets with enough computational power to make completely autonomous decisions.

How would this change military strategy?

Imagine dis-mounted warfighters with state-of-the-art communications and ISR capabilities without the need to carry heavy battery loads?

How might this change operational thinking?

Well, to make such visions a reality requires breakthrough progress in ultra-low power electronics.

Clearly, powerful digital computation capabilities are the key to realizing these visions for the military capabilities of tomorrow.

*What is limiting us from achieving these goals?*

The worldwide semiconductor industry has realized remarkable advances over the past several decades with the progress defined by Moore's Law.

So what is the problem?

Why should DARPA get involved here?

How can we help drive progress in ultra-low power digital electronics?

Well, Moore's Law has come under serious strain over the past several years.

The main issue is power density.

Device scaling has reached the point where the leakage power can no longer be controlled.

In fact, classical transistor scaling is coming to an end due to power

dissipation limitations.

To be sure, increases in device density are still occurring, but the incremental performance improvement is decreasing with new technologies.

This fact is driving the transition from increasing IC clock frequency to increasing the number of logic “cores” per IC, in an attempt to squeeze out further performance increases.

This multi-core architecture is shown here, where a single very fast CPU filling the whole chip is replaced by multiple smaller and slower CPU's each filling only part of the chip.

Even for multi-core IC architectures, power dissipation is still an important problem.

So the key challenge for modern electronics is developing technologies with unprecedented levels of power efficiency.

This ultra-low power electronics vision will rely on such breakthroughs -- so why not simply wait for Industry to solve the power problem?

Well, the answer is that historical electronics progress has been achieved by a well defined process of so called “classical” device scaling.

Each new technology certainly required new processes and equipment to be developed, but the methods for scaling were well-known and the risks manageable.

Nevertheless, the power dissipation crisis we face today cannot be solved by the “classical” scaling approaches used in the past.

*I believe that substantial further progress **IS** possible in the power efficiency realm!*

We have **NOT** reached the physical limits for the energy required to perform a computation and I'd like to explain why.

The energy scale to perform a computation is of the order of the thermal energy which is approximately 25 meV at room temperature.

To do this computation with acceptable signal-to-noise ratios requires several times this value.

Let's say 100 meV.

Today's most advanced CMOS runs at 1 volt.

This means that we are a factor of 10 away from the physical limit.

Since active power scales as the square of the voltage supply, we are actually a factor of 100 away from the physical limit.

This is a significant opportunity for progress.

What are some revolutionary ideas that might enable us to approach the physical limits for computational energy consumption?

We are looking at several possible approaches and I'm interested in your ideas on how we can achieve, for example, a 100 meV transistor.

One approach is to make electronic switches that look more like a step

function.

Steeper turn-on slopes enable much lower applied voltages without a performance penalty.

Very steep turn-on slopes are not physically possible using the types of CMOS devices we use today.

New physics is required to develop “non-thermionic” switches, which can have much steeper turn-on slopes.

We are starting to explore such devices based on gate-modulated tunneling barriers in contrast to today’s gate-modulated thermal barrier switches.

Significant innovations will be required in both device physics and possibly materials but, with your help and new ideas, this goal should be within reach.

Another approach involves the development of a radically new material system based on very thin sheets of carbon atoms called “graphene”.

Note that only a single atomic layer is involved with a thickness of less than 1 nm.

Electrons in such materials move with very little resistance and can therefore be modulated with very low applied voltages.

But the materials technology is at a very early stage of development.

We have a new program targeting the development of the graphene material system to make very low power switches and amplifiers.

But the ultimate goal, again with your help,  
is to achieve close integration into the mainstream silicon process.

We are currently working on a number of aggressive program efforts  
aimed at dramatically lowering the power dissipation for computation.

*But this is not the whole story!*

I still need to tell you about the other key component involved in power  
dissipation: the leakage or standby power.

At any given time,  
many circuits are not performing computations, so this component of  
power dissipation is important.

In fact, the leakage power has been increasing at an alarming rate with  
new technologies.

This is due to the breakdown of “classical” CMOS scaling.

Leakage power is becoming as important as active computational power  
for today’s advanced technologies.

To realize the vision of ultra-low power, breakthroughs must be  
achieved to reign in the leakage power in advanced electronics.

So, how can we deal with this problem?

Well, one possible approach is to *use subthreshold leakage currents* to  
do the desired computation.

We explored this approach in one of our recent efforts.

The devices are operated at such low voltages that the currents were all due to subthreshold leakage.

In this ultra-low voltage regime, the applied voltages are well below the device threshold.

But this operation mode comes with a significant penalty; greatly reduced currents which translate into greatly reduced performance.

The main challenge of this research is to achieve ultra-low power computation with reasonable performance.

We are currently exploring subthreshold performance enhancement by making use of algorithmic parallelism.

This approach essentially trades off increased circuit area for dramatically improved power efficiency.

Another approach for achieving revolutionary power efficiency in a totally different way;  
is to use novel  
3-dimensional architectures.

Today's ICs consist of a single layer of active devices and are thus referred to as  
2-dimensional.

Building a technology with multiple layers of active devices opens up entirely new architectural opportunities.

Much more computational power can be placed per unit volume, significantly lowering resulting footprints.

Each layer, or “tier”, can be densely interconnected to the next... which will significantly increase the interconnect bandwidth.

Each tier could also have a specialized function, such as logic, memory or analog, with extremely-dense area interconnects to the next tier.

Mapping important algorithms into a 3-dimensional topology offers a whole new degree of freedom for optimizing power efficiency.

The combination of 3D architectures, with ultra-low power device technologies, offers the promise of a dramatic increase in efficient computational power per unit volume.

Unattended sensors with unlimited lifetimes...

unmanned air vehicles navigating using vision...

dis-mounted warfighters with state-of-the-art communications and ISR present compelling visions for the military of the future.

Achieving such ambitious goals will *require breakthroughs in power efficient electronics.*

To make this ambitious vision a reality, we need your ideas in this area .

I urge you all to think about this problem;  
you never know where the next breakthrough will come from.

I would now like to introduce Dr. Jag Shah who will discuss his vision for solving the intra-chip communications bottleneck problem.